



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,980	03/01/2002	Osman Kent	TD-168	6304

29106 7590 01/12/2006

GROOVER & HOLMES
BOX 802889
DALLAS, TX 75380-2889

EXAMINER

TUNG, KEE M

ART UNIT PAPER NUMBER

2671

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

MAILED

JAN 12 2006

Technology Center 2600

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/086,980
Filing Date: March 01, 2002
Appellant(s): KENT, OSMAN

Patrick C. R. Holmes
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/21/05.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Claimed Subject Matter*

The summary of claimed subject matter contained in the brief is correct.

(6) *Grounds of Rejection to be Reviewed on Appeal*

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) *Claims Appendix*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) *Evidence Relied Upon*

6,025,853	Baldwin	2-2000
5,459,864	Brent et al	10-1995

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3-5 and 7-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin (6,025,853) in view of Brent et al (5,459,864).

Baldwin teaches a graphics processor (2E) comprising a plurality of parallelized graphics computational units (col. 64, lines 16-21, 25-29 and 38-40), such as, rasterizer, scissor, stipple, alpha test, fog, texture, stencil test, depth test, local and frame buffer controllers. However, Baldwin fails to explicitly teach or suggest one or more task allocation units programmed to bypass defective ones of said subunits within said groups, and distribute incoming tasks only among operative ones of said subunits. It is old and well known and well used in the art to dynamically load balanced among multiple processors include skip or bypass defective unit(s). Furthermore, Brent teaches a load balancing, error recovery and reconfiguration control in a data movement subsystem with cooperating plural queue processors (Fig. 2, abstract, col. 2, lines 39-45, col. 5, lines 49-52 and col. 6, lines 11-18). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of bypass defective unit and distribute load from defective unit to other units

of Brent into the system of Baldwin in order to automatic load balancing among plural processors, automatic recovery from any failing processor, and automatic reconfiguration for the subsystem containing the processors without intervention from the operating system as taught by Brent (col. 1, lines 18-24). Therefore, at least claims 1, 3-5 and 7 would have been obvious.

As per claims 8 and 9, Baldwin teaches one or more of said parallelized graphics computational units operate with no more than 4 operative vertex processors and/or texture pipelines (Fig. 2D).

As per claims 10 and 11, Baldwin further teaches shading unit (col. 48, lines 26-50), primary texture cache (local texture storage, col. 7, lines 25-31) and a texture filter unit (col. 48, line 53 to col. 49, line 63).

Claims 12-19 are similar in scope to claims 1, 3-5 and 7-11, and thus are rejected under similar rationale.

Claims 20-27 are similar in scope to claims 1, 3-5 and 7-11, and thus are rejected under similar rationale.

Claims 28-35 are similar in scope to claims 1, 3-5 and 7-11, and thus are rejected under similar rationale.

(10) Response to Argument

It is noted that the groups A, B, C and D referred in the Brief is treated as the groups indicated in the previous filed Brief dated 3/4/05. Claims 1, 3-5 and 7-11 referred to as group A; claims 12-19, 20-27 and 28-35 referred to as groups B, C and D, respectively.

First, appellant argues that Brent's teaching deals with the allocation between separate processors within a data move subsystem, while Baldwin deals with the allocation within a single graphics processor chip having a plurality of units. However, the examiner has failed to address the unique limitations of "*a graphics processor ... with one or more task allocation units programmed to bypass defective ones of said units*". The examiner disagrees. As shown in the detail rejection above, the examiner incorporated the teachings of "programmed to bypass defective ones of units" of Brent (see col. 6, lines 33-37, **logically removed** (or bypass) defective processor from the subsystem) into the single graphics chip having multiple computation units (it is note that a computation unit can be considered as a processor to one of ordinary skill in the art) of Baldwin in order to automatic load balancing among plural processors (or units), automatic recovery from any failing processor, and automatic reconfiguration for the subsystem containing the processors without intervention from the operating system as taught by Brent (col. 1, lines 18-24). It is well known and well used in the patent applications, specially in patent claims, a processor, a computation unit, a processing unit, and a controller, etc ... are interchangeable in the art and all can be called as a processor. Each component can vary in size and the scale of the component can all be different. It all depends on how the claims have being written and as long as it is clear. In the present application, the important issue is what the Brent reference as a whole teaches to one of ordinary skill in the art (allocation between multiple processors/units) in place of Baldwin.

In the present application, the prior art to Baldwin (same assignee) deals with allocation within a single graphics processor comprising a plurality of computational **units** (such as, a vertex **processor** in claim 3) and the prior art to Brent deals with allocation between pluralities of processors (in the place of vertex processor). However, as is well known in the art, a computation unit can be considered as a processor. There is no uniform definition which one is bigger. What is important to one of ordinary skill in the art is what the teachings as whole of Brent suggest to one of ordinary skill in the art, whether it is among a plurality of **processors** or a plurality of **units**? Therefore, appellant's arguments related to Baldwin deals with a single processor and Brent deals with multiple processors are not deemed to be persuasive even in view of appellant's own patent (A graphics processor comprising multiple vertex **processors** in claim 3).

Secondly, appellant argues that there is no teachings or suggestion in the cited references to combine the cited references. The examiner disagrees. As can be seen from the rejection above and the prior art, Baldwin teaches allocation between multiple units/processors and Brent also teaches allocation between multiple processors/units. Brent further teaches or suggests that his invention provides all the benefits and advantages over the prior art system which did not have the feature of distribute, recovery from defective units by reconfiguration of the system (see col. 1, lines 18-24).

Thirdly, appellant argues that the cited prior art fails to teach or suggest a single processor may continue to function even though it is partially defective. Brent clearly teaches this feature (See abstract, Figs. 2 and 11; col. 5, line 33 to col. 6, line 49; and col. 14, line 64 to col. 18, line 30).

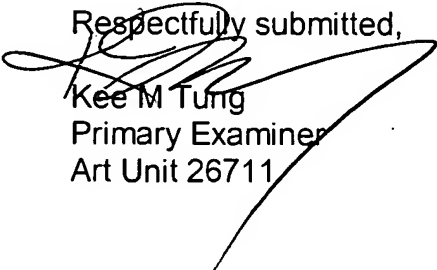
Lastly, all the arguments also apply to Group B, C and D (there is no additional arguments for these Groups).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,


Kee M Tung
Primary Examiner
Art Unit 26711

December 20, 2005

Conferees

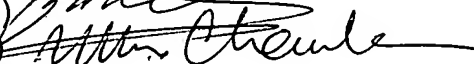
Matthew Bella (SPE)

Bipin Shalwala (SPE)

Ulka Chauhan (SPE)







MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Groover & Holmes
P.O. Box 802889
Dallas, TX 75380
Tel: 972.980.5840
Fax: 972.980.5841